ABSTRACT OF THE DISCLOSURE

Clock signals and digital data signals at a variable frequency are introduced to the input of a FIFO and are passed from the FIFO at a second (or intermediate) frequency controlled by a numerically controlled oscillator. To regulate the frequency of the signals from the numerically controlled oscillator, the phases of the clock signals at the variable frequency are compared in a phase detector with the phases of the signals from the numerically controlled oscillator to generate an error signal. The error signals and the signals at a fixed sampling frequency higher than the intermediate frequency regulate the frequency of the signals from the numerically controlled oscillator and thus the frequency of the digital data signals from the FIFO. The digital data signals from the FIFO are converted to a pair of signals at the second frequency. The pair of signals at the second frequency have individual ones of a plurality of analog levels dependent upon a code indicated by successive pairs of the digital data signals. The signals at the second (or intermediate) frequency modulate a pair of trigonometrically related signals at the fixed sampling frequency. The modulated signals at the fixed sampling frequency are combined and the combined signals are sampled at the fixed sampling frequency to corresponding analog values by a digital-to-analog converter.

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